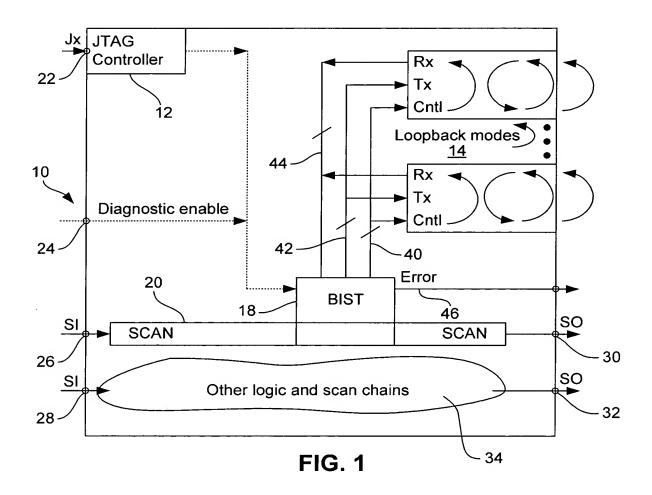


## Inventor: Antonio Marriog Martinez Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD

Attorney: Guy K. Clinger (303) 298-9888 PDNO: 10030374-1

Sheet 1 of 5



### Inventor: Antonio Marriog Martinez Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD Attorney: Guy K. Clinger (303) 298-9888 PDNO: 10030374-1

#### Sheet 2 of 5

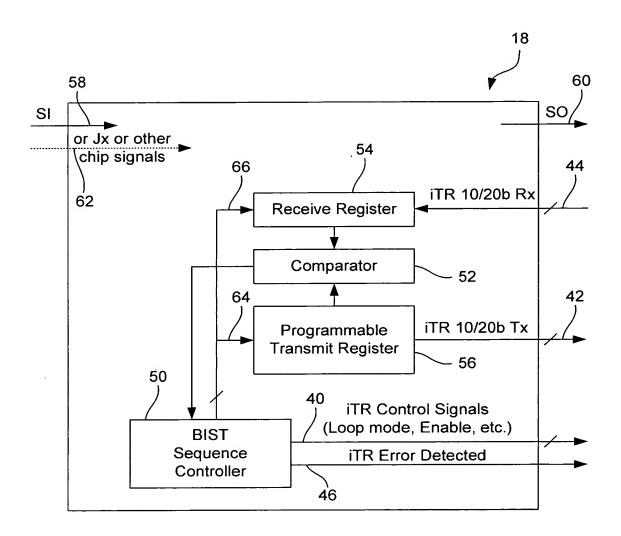


FIG. 2

# Inventor: Antonio Marriog Martinez Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER CIRCUITS AND METHOD Attorney: Guy K. Clinger (303) 298-9888 PDNO: 10030374-1

### Sheet 3 of 5

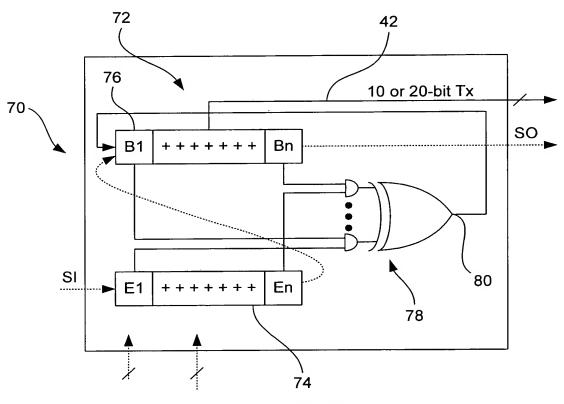


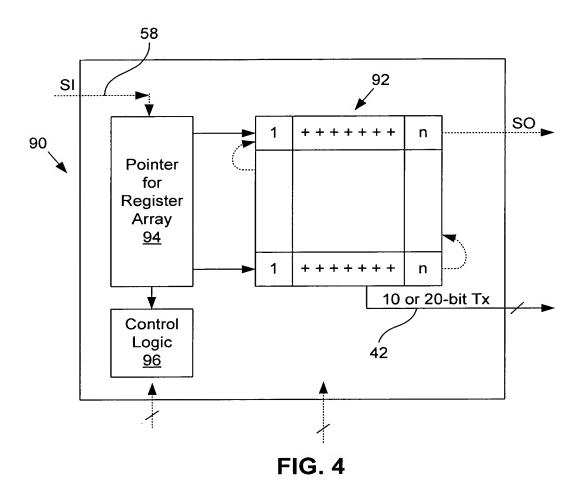
FIG. 3

Inventor: Antonio Marriog Martinez

Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER

CIRCUITS AND METHOD Attorney: Guy K. Clinger (303) 298-9888 PDNO: 10030374-1

### Sheet 4 of 5



### Inventor: Antonio Marriog Martinez Title: PROGRAMMABLE BUILT-IN SELF-TEST CIRCUIT FOR SERIALIZER/DESERIALIZER **CIRCUITS AND METHOD** Attorney: Guy K. Clinger (303) 298-9888

PDNO: 10030374-1

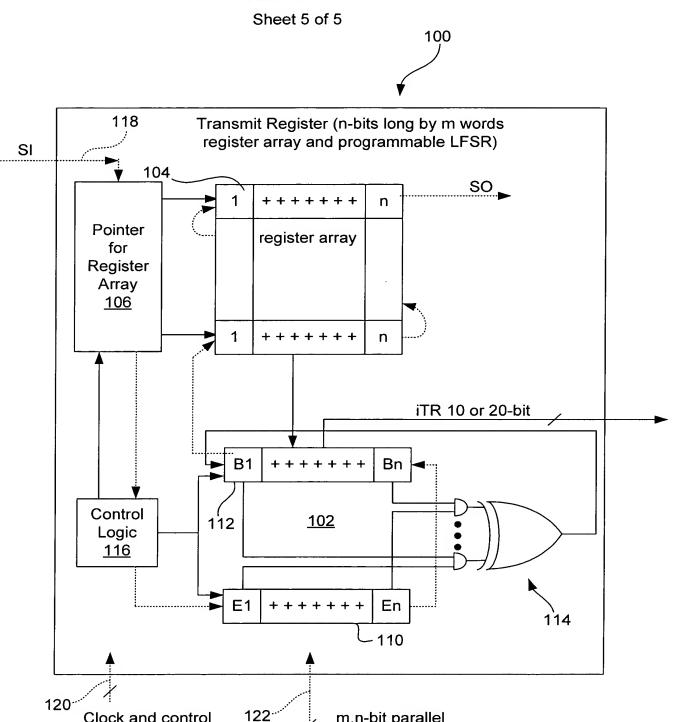


FIG. 5

m,n-bit parallel bus to Register

Array and Pointer

Clock and control

signals to load register array and